XR-U550/U550RDS/U551RDS
XR-U660/U660RDS/U661RDS

SERVICE MANUAL

US Model
Canadian Model
XR-U550

AEP Model
XR-U550RDS/U551RDS
XR-U660RDS/U661RDS

UK Model
XR-U551RDS/U661RDS

E Model
XR-U550/U660

Photo: XR-U660RDS

Model Name Using Similar Mechanism	XR-7130/7140/7142/7600
Tape Transport Mechanism Type	MG-55N-31/55N2-31

SPECIFICATIONS

Cassette player section

Tape track: 4-track 2-channel stereo

Frequency response:
XR-U550/U550RDS/U551RDS
30 – 18,000Hz
XR-U660/U660RDS/U661RDS
30 – 20,000 Hz

Signal-to-noise ratio

Cassette type	Dolby B	Dolby C	Dolby NR off
TYPE II, IV	66 dB	76 dB	58 dB
TYPE I	63 dB	73 dB	55 dB

Wow and flutter: 0.09% (WRMS)

Tuner section

FM

Tuning range:
XR-U550
87.9 – 107.9 MHz
XR-U550RDS/U551RDS/U660/U660RDS/U661RDS
87.5 – 108.0 MHz

Antenna terminal: External antenna connector

Intermediate frequency: 10.7 MHz

Usable sensitivity: 12 dBf (75 ohms)

Selectivity: 75 dB at 400 kHz

Signal-to-noise ratio: 65 dB (stereo), 70 dB (mono)

Harmonic distortion at 1 kHz: 0.5% (stereo), 0.3% (mono)

Separation: 35 dB at 1 kHz

Frequency response: 30 – 15,000 Hz

Capture ratio: 2 dB

AM (MW/LW)

Tuning range:
XR-U550
530 – 1,710 kHz
XR-U550; E/U660
530 – 1,620 kHz (at 10 kHz step)
XR-U550; E/U550RDS/U660/U660RDS
531 – 1,602 kHz
AM tuning interval
9 kHz/10 kHz switchable
(except the model for European countries)
XR-U551RDS/U661RDS
MW: 531 – 1,602 kHz
LW: 153 – 281 kHz

– Continued on next page –

FM/AM CASSETTE CAR STEREO
XR-U550/U550RDS/U660/U660RDS
FM/MW/LW CASSETTE CAR STEREO
XR-U551RDS/U661RDS

使用時は添付資料も参照のこと
Refer to the additional documents.

SONY®

SECTION 4
DIAGRAMS

4-1. PIN DESCRIPTIONS
Master Microcomputer IC501 (μPD75116GF-F41-3BE)

<table>
<tr><th>Pin No.</th><th>Name</th><th>I/O</th><th>Description</th></tr>
<tr><td>63</td><td>POS 3</td><td>I</td><td rowspan="4">Mechanism Deck Position Detection pin.

(See the table below.)
*(With tape rotation in normal direction)
<table>
<tr><th></th><th>EJECT</th><th>STOP</th><th>←</th><th>FF</th><th>←</th><th>REW</th><th>←</th><th>PLAY</th></tr>
<tr><td>POS 0</td><td>L</td><td>L</td><td>L</td><td>H</td><td>H</td><td>H</td><td>H</td><td>H</td></tr>
<tr><td>POS 1</td><td>H</td><td>H</td><td>L</td><td>L</td><td>L</td><td>H</td><td>H</td><td>H</td></tr>
<tr><td>POS 2</td><td>H</td><td>H</td><td>H</td><td>H</td><td>L</td><td>L</td><td>L</td><td>H</td></tr>
<tr><td>POS 3</td><td>L</td><td>H</td><td>H</td><td>H</td><td>H</td><td>H</td><td>L</td><td>L</td></tr>
</table>
H : High input, L : Low input</td></tr>
<tr><td>64</td><td>POS 2</td><td>I</td></tr>
<tr><td>1</td><td>POS 1</td><td>I</td></tr>
<tr><td>2</td><td>POS 0</td><td>I</td></tr>
<tr><td>3</td><td>LINK OFF</td><td>O</td><td>Not used.</td></tr>
<tr><td>4</td><td>AMP ON</td><td>O</td><td>Not used.</td></tr>
<tr><td>5</td><td>POWER-ON</td><td>O</td><td>Power ON/OFF Output pin. Set this output "High" to turn power on. Set it "Low" to turn all power off.</td></tr>
<tr><td>6</td><td>ACC-ON</td><td>O</td><td>Button Illumination Power ON/OFF Output pin. Set this output "High" to turn the power on.</td></tr>
<tr><td>7</td><td>$\overline{\text{RESET}}$</td><td>I</td><td>Reset pin.</td></tr>
<tr><td>8</td><td>X2</td><td>—</td><td rowspan="2">Connection pin for System Clock Oscillation. 4.19MHz connection.</td></tr>
<tr><td>9</td><td>X1</td><td>I</td></tr>
<tr><td>10</td><td>DM CLOSE</td><td>O</td><td rowspan="2">Not used.</td></tr>
<tr><td>11</td><td>DM OPEN</td><td>O</td></tr>
<tr><td>12</td><td>$\overline{\text{SYSTEM RESET}}$</td><td>O</td><td>Pin which resets all of slave microcomputers that are connected and are communicating on the UNILINK BUS. Switching this output from "Low" to "High" level causes resetting. Usually it is kept "High".</td></tr>
<tr><td>13</td><td>SYNC</td><td>O</td><td>Pin which outputs the pulse for determining timing of communication to data line. (UNILINK BUS interface SYNC pin)</td></tr>
<tr><td>14</td><td>MUTE</td><td>O</td><td>Output pin used to enable Audio Muting. This output is kept "High" during audio muting.</td></tr>
<tr><td>15</td><td>CLK VOL</td><td>O</td><td>Pin for Clock Output to the electronics VOL IC (IC 321: LC7537AN).</td></tr>
<tr><td>16</td><td>DATA VOL</td><td>O</td><td>Pin for Data Output to the electronics VOL IC.</td></tr>
<tr><td>17</td><td>CE VOL</td><td>O</td><td>Pin for CE Output to the electronics VOL IC. This output is used as the latch signal to send data.</td></tr>
<tr><td>18</td><td>NOSE</td><td>I</td><td>Initialization pin which determines whether the nose is removed or not. When this input is "High", there are no nose removal failure caution alarm, no cassette EJECT and no nose open function (by means of pressing OPEN button for two sec).</td></tr>
<tr><td>19</td><td>B/C (INT)</td><td>I</td><td>Initialization pin which determines whether Dolby B NR only or Dolby B and C NR. When "Low", this input sets both B and C. When "High", it sets B only.</td></tr>
</table>

<table>
<tr><th>Pin No.</th><th>Name</th><th>I/O</th><th>Description</th></tr>
<tr><td>20</td><td>$\overline{\text{CLOCK}}$</td><td>I</td><td>Initialization pin which determines whether the internal clock is present or not. When "Low", this input initializes the system with the clock present.</td></tr>
<tr><td>21</td><td>POWER SELECT</td><td>I</td><td>Power Select switch (initialization). Set this input "Low" to select Power select OFF setting (to cope with cars without accessary position).</td></tr>
<tr><td>22</td><td>PL</td><td>O</td><td>MD Plunger Control pin.</td></tr>
<tr><td>23</td><td>CM</td><td>O</td><td>MD Capstan Motor Control pin.</td></tr>
<tr><td>24</td><td>LM−</td><td>O</td><td rowspan="2">MD Loading Motor Control pin</td></tr>
<tr><td>25</td><td>LM+</td><td>O</td></tr>
<tr><td></td><td></td><td></td><td><table><tr><th>LM− / LM+</th><th>High</th><th>Low</th></tr><tr><td>High</td><td>Brake</td><td>Loading Direction</td></tr><tr><td>Low</td><td>Eject Direction</td><td>Stopped</td></tr></table></td></tr>
<tr><td>26</td><td>Vss</td><td>—</td><td>Vss pin.</td></tr>
<tr><td>27</td><td>DP 0</td><td>I</td><td rowspan="2">Not used. Pullup H.</td></tr>
<tr><td>28</td><td>DP 1</td><td>I</td></tr>
<tr><td>29</td><td>NSW</td><td>I</td><td>Nose Presence Detection pin. When "Low", this input indicates that the nose is removed.</td></tr>
<tr><td>30</td><td>CSW</td><td>I</td><td>Cassette Tape Presence Detection pin. When "High", this input indicates that cassette tape is present.</td></tr>
<tr><td>31</td><td>REEL 1</td><td>I</td><td>Cassette Tape Rotation Detection pin (this input indicates Take up side when tape is being rotated in normal direction).</td></tr>
<tr><td>32</td><td>REEL 2</td><td>I</td><td>Cassette Tape Rotation Detection pin (this input indicates Supply side when tape is being rotated in normal direction).</td></tr>
<tr><td>33</td><td>F/$\overline{\text{R}}$</td><td>I</td><td>Cassette Tape Run Direction Detection pin. When "Low", this input indicates REVERSE.</td></tr>
<tr><td>34</td><td>——</td><td>—</td><td>Not used. (Connected to GND.)</td></tr>
<tr><td>35</td><td>——</td><td>—</td><td>Not used. (Connected to GND.)</td></tr>
<tr><td>36</td><td>——</td><td>—</td><td>Not used. (Connected to GND.)</td></tr>
<tr><td>37</td><td>CLK OUT</td><td>O</td><td>Serial Communication Clock Output pin. (UNILINK BUS Interface Clock Output pin)</td></tr>
<tr><td>38</td><td>$\overline{\text{BUS ON}}$</td><td>O</td><td>UNILINK BUS Interface Bus ON Output terminal. Set this output "Low" to enable communication on the bus.</td></tr>
<tr><td>39</td><td>KEY RESET</td><td>O</td><td>Pin which resets the KEY DISPALY mircocomputer (IC 702).</td></tr>
<tr><td>40</td><td>BEEP</td><td>O</td><td>BEEP Output pin.</td></tr>
<tr><td>41</td><td>SI</td><td>I</td><td>Serves as both Serial Data Input pin and Detection pin for Communication Request from slave. (UNILINK BUS Interface Data Input pin)</td></tr>
</table>

Pin No.	Name	I/O	Description
42	SO	O	Serial Data Output pin. (UNILINK BUS Interface Data Output pin)
43	CLK IN	I	Serial Communication Clock Input pin.
44	BU CHECK	I	Power Voltage Detection pin.
45	$\overline{\text{ACC CHECK}}$	I	Accessory Voltage Detection pin. When "High", this input indicates ACC OFF.
46	$\overline{\text{TEL MUTE}}$	I	Pins which detects a telephone call. This input becomes "Low" to mute −20dB audio signal. It becomes "High" to return the signal to its original VOL level.
47	———	—	Not used. (Connected to GND.)
48	$\overline{\text{TV}}$/TV1,2	I	Intialization pin for the number of bands (preset count) for TV when the Hide-away TV tuner is connected. When "Low", this input sets 1 band (preset count to 10). When " High", it sets 2 bands for TV1,TV2 (preset count to 20).
49	$\overline{\text{KEY 5V}}$	O	Power Control pin for the KEY DISPALY microcomputer. Set this output "Low" to turn the power on.
50	$\overline{\text{AUX ON}}$	O	This output is "Low" when supplied as an external input of UNILINK IN AUDIO to CD, TV, etc. It supplies high impedance to other destinations.
51	$\overline{\text{D ON}}$	O	This output is "Low" when sound is being produced from cassette tape. Ohterwise, it supplies high impedance.
52	———	—	Not used.
53	———	—	Not used.
54	ANT ON	O	This output supplies high impedance when the tuner or TV is on. It is "Low" when any other source is on.
55	———	—	Not used.
56	———	—	Not used.
57	NC	—	Connected to VDD.
58	V_{DD}	—	V_{DD} pin.
59	B/C	O	This output is "High" when Dolby B NR is on. It is "Low" output when C NR is on.
60	DNR ON	O	This output is "Low" when Dolby NR is on. It is "High" when Dolby NR is off.
61	$\overline{\text{AMS IN}}$	I	Detection pin which determines whether tape sound is present or not. This input is "Low" when tape sound is present.
62	MTL	I	Tape $\overline{\text{NORMAL}}$/METAL Detection pin. This input is "Low" when normal tape is used.

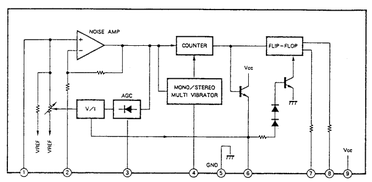
Key Display Microcomputer IC702 (μPD75008GB-676-3B4)

Pin No.	Name	I/O	Description
44	KI7	I	KEY SCAN Input pin.
1	KI6	I	
2	KI5	I	
3	KI4	I	
4	KI3	I	
5	KI2	I	
6	KI1	I	
7	KI0	I	
8	KO3	O	KEY SCAN Output pin.
9	KO2	O	
10	KO1	O	
11	KO0	O	
12	NC	—	(Connected to VDD.)
13	———	—	Not used.
14	———	—	
15	———	—	
16	———	—	
17	V_{SS}	—	V_{SS} pin.
18	XT1	—	(Connected to GND.)
19	XT2	—	Not used.
20	$\overline{\text{RESET}}$	I	Reset pin.
21	X1	I	Connection pin for System Clock oscillation. 4.19MHz connection.
22	X2	—	
23	LCD CLK	O	Pin for Clock Output to LCD DRIVER IC (IC 703: TC9240F)
24	LCD DATA	O	Pin for Data Output to LCD DRIVER IC.
25	LCD CE	O	Pin for CE Output to LCD DRIVER IC. This output is used as the latch signal to send data.
26	LCD INH	O	Pin for INH Output to LCD DRIVER IC.
27	LINK OFF	O	Not used.
28	REQ	O	UNILINK BUS Interface Request pin. This pin is "High" to request communication from the master microcomputer (IC 501).
29	DATA IN	I	Serves as both Serial Data Input pin and Detection pin for Communication Request from slave. (UNILINK BUS Interface Data Input pin)
30	DATA OUT	O	Serial Data Output pin. (UNILINK BUS Interface Data Output pin)
31	CLK IN	I	Serial Communication Clock Input pin. (UNILINK BUS Interface Clock Input pin)
32	BU CHECK	I	Power Voltage Detection pin.
33	———	—	(Connected to GND.)
34	NC	—	(Connected to VDD.)
35	$\overline{\text{TV CONT}}$	I	Not used.
36	$\overline{\text{BUS ON}}$	I	UNILINK BUS Interface Bus ON Terminal. When this output is "Low", communication on the bus is enabled.

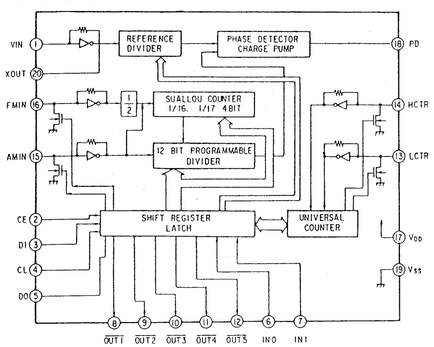
Pin No.	Name	I/O	Description
37	SIRCS	I	Infrared Remote Control Input pin.
38	NC	—	(Connected to V_{DD}.)
39	V_{DD}	—	V_{DD} pin.
40	LCD ON	O	LCD Back Illumination and LCD DRIVER IC Power Control pin.
41	ACC-ON ILL	O	Button Illumination Output for function keys. This output is "High" when ACC is ON and it is "Low" when ACC is OFF (with Power Select switch selected ON).
42	P-ON ILL	O	Button Illumination Output pin for buttons other than function keys. This output is "High" when power is turned on and it is "Low" when power is turned off.
43	COLOR	O	Illunimation Color Select Output pin. Set this output "High" to select Green. Set it "Low" to select Amber.

• IC Block Diagrams

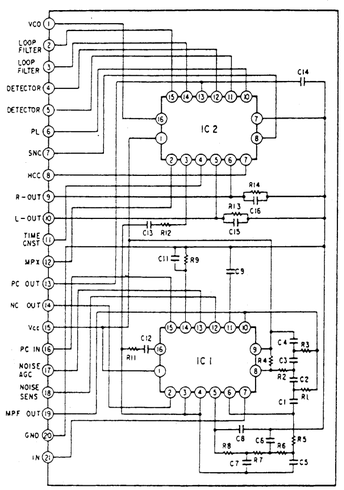
IC1 LA1060



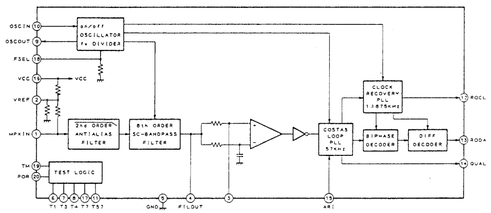
IC2 LC7216M



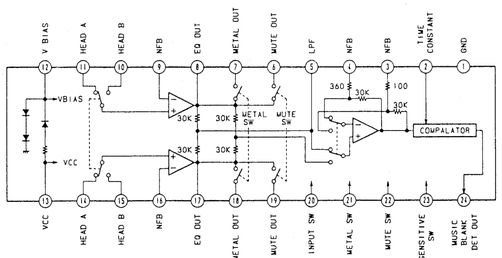
IC3 STK-3400



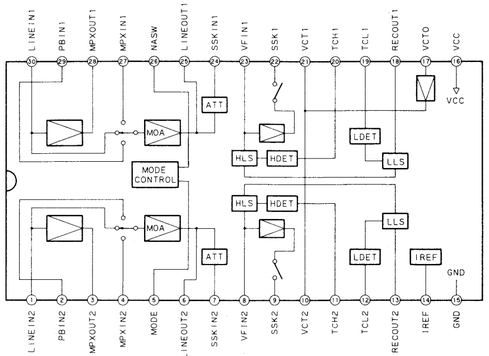
IC4 TDA7330



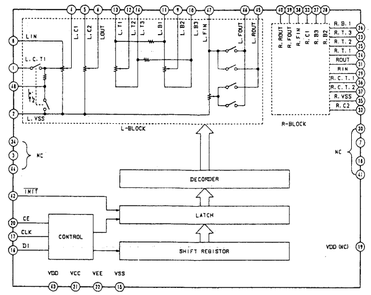
IC301 BA3430FS



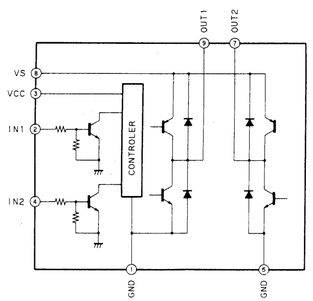
IC311 CXA1332M



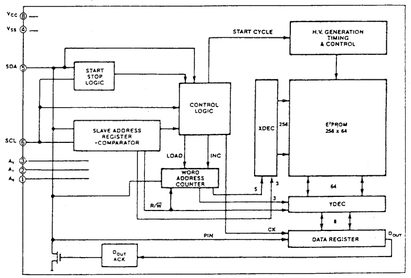
IC321 LC7537AN



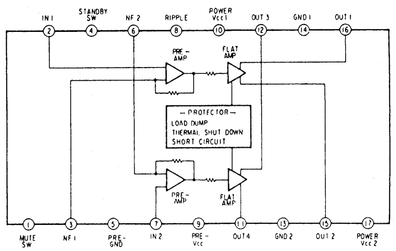
IC431 LB1638



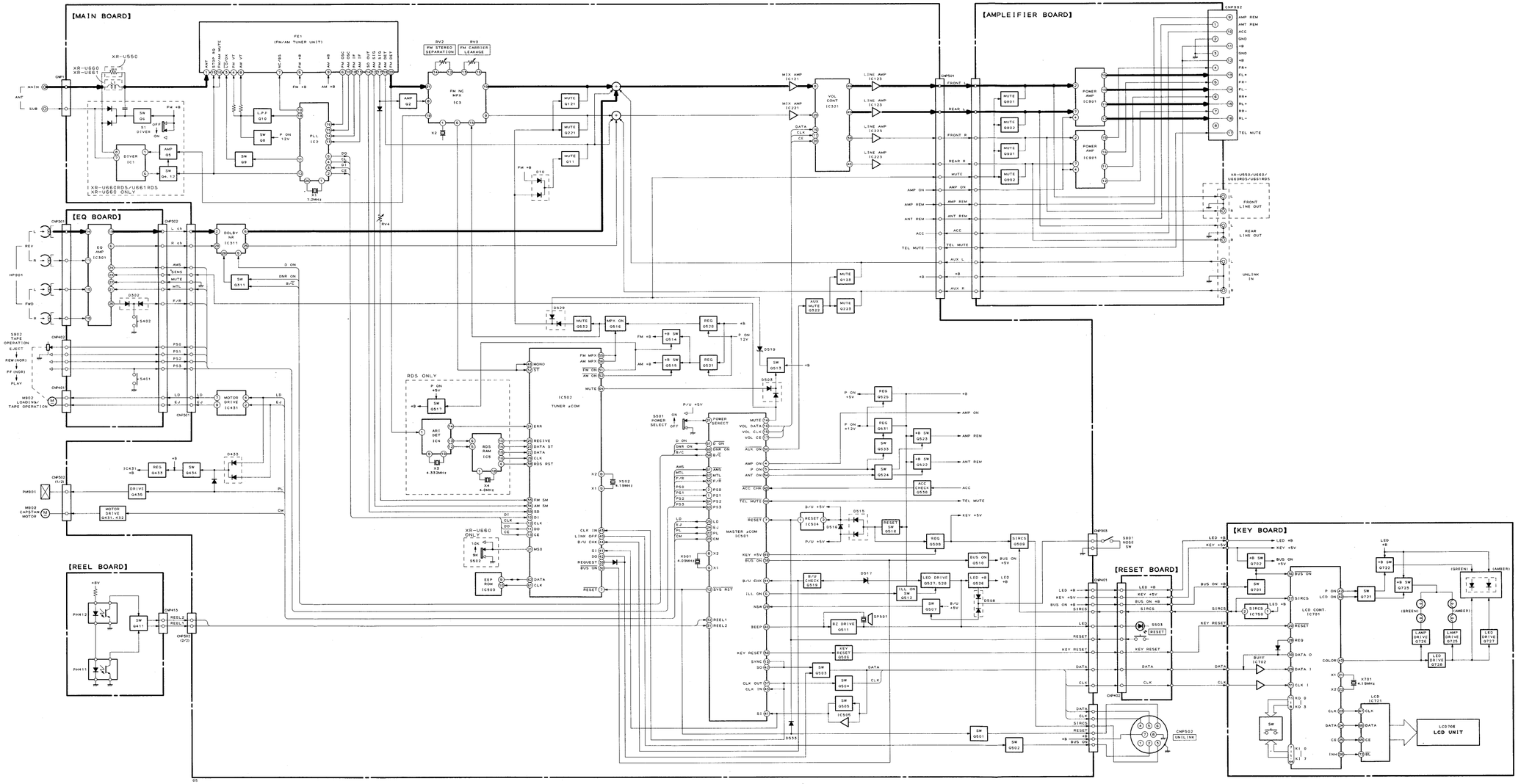
IC503 X24C16SI



IC801, 901 TA8215H

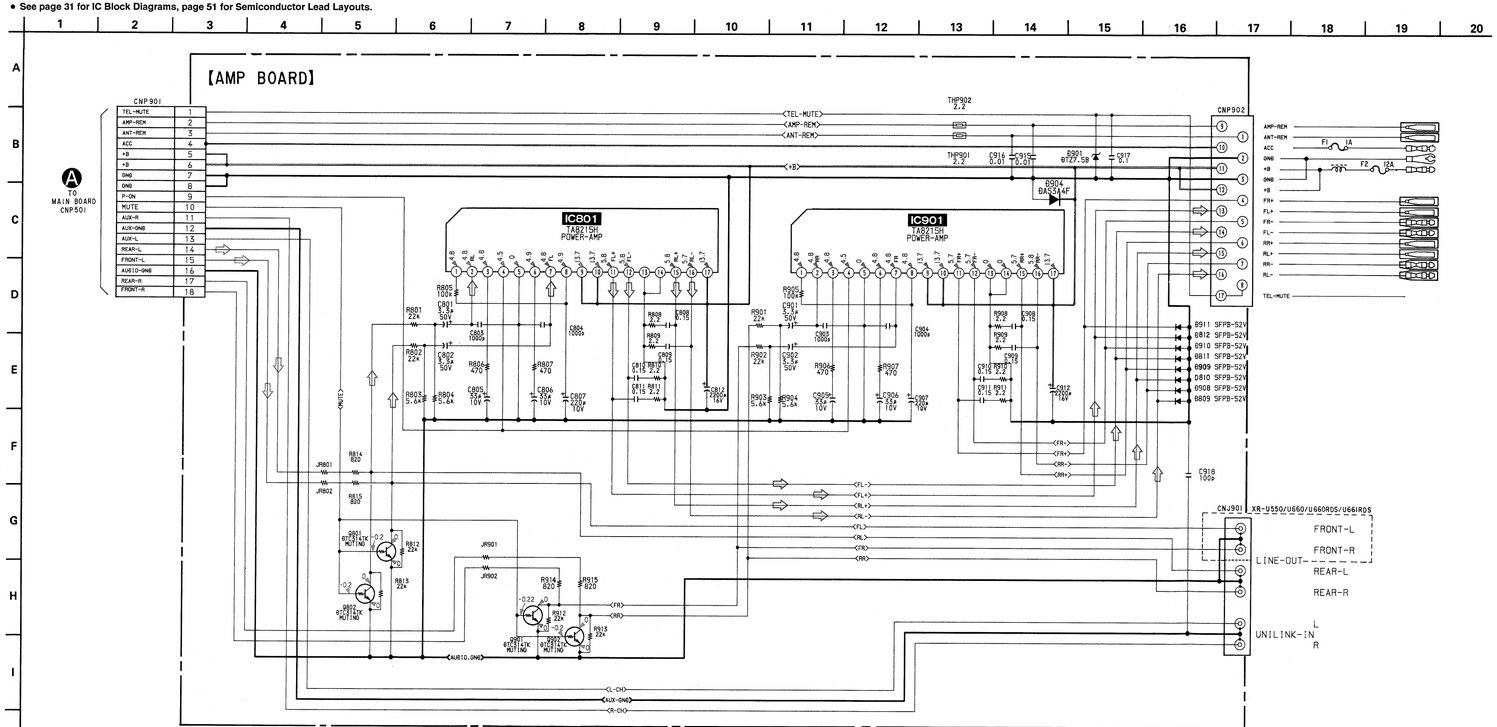


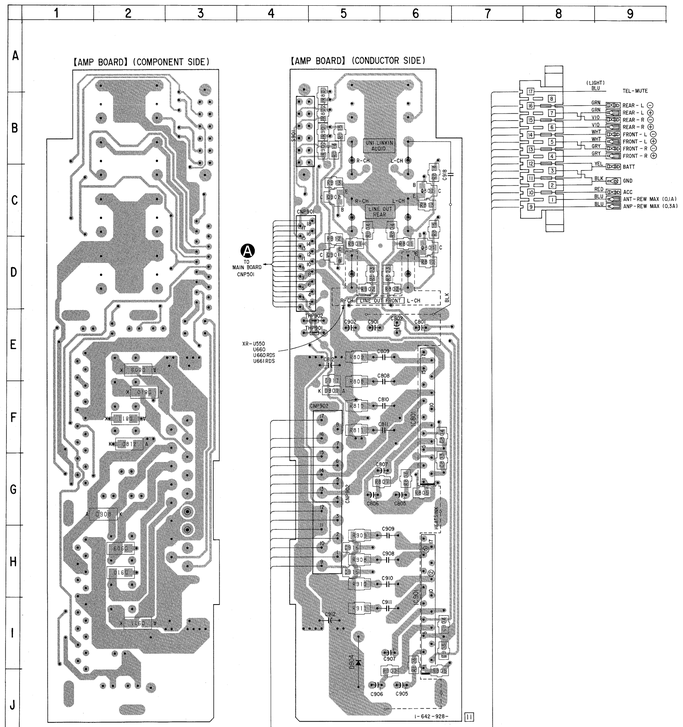
4-2. BLOCK DIAGRAM



4-3. PRINTED WIRING BOARDS AND SCHEMATIC DIAGRAM (AMP SECTION)

• See page 31 for IC Block Diagrams, page 51 for Semiconductor Lead Layouts.





• **Semiconductor Location**

Ref. No.	Location
D809	E-2
D810	F-2
D811	F-2
D812	F-2
D908	G-2
D909	H-2
D910	H-2
D911	I-2
IC801	F-6
IC901	I-6
Q801	D-6
Q802	C-6
Q901	D-5
Q902	C-5

Note on Schematic Diagram:

- All capacitors are in μF unless otherwise noted. pF: μμF 50 WV or less are not indicated except for electrolytics and tantalums.
- All resistors are in Ω and ¼ W or less unless otherwise specified.
- % : indicates tolerance.
- ═══ : B + Line.
- Power voltage is dc 14.4 V and fed with regulated dc power supply from BAT and ACC terminals.
- Voltages and waveforms are dc with respect to ground under no-signal (detuned) conditions.
  no mark : PB
  ( ) : STOP
- Signal path.
  ⇨ : PB

Note on Printed Wiring Board:

- o—— : parts extracted from the component side.
- ● : Through hole.
- ▒▒▒ : Pattern from the side which enables seeing.

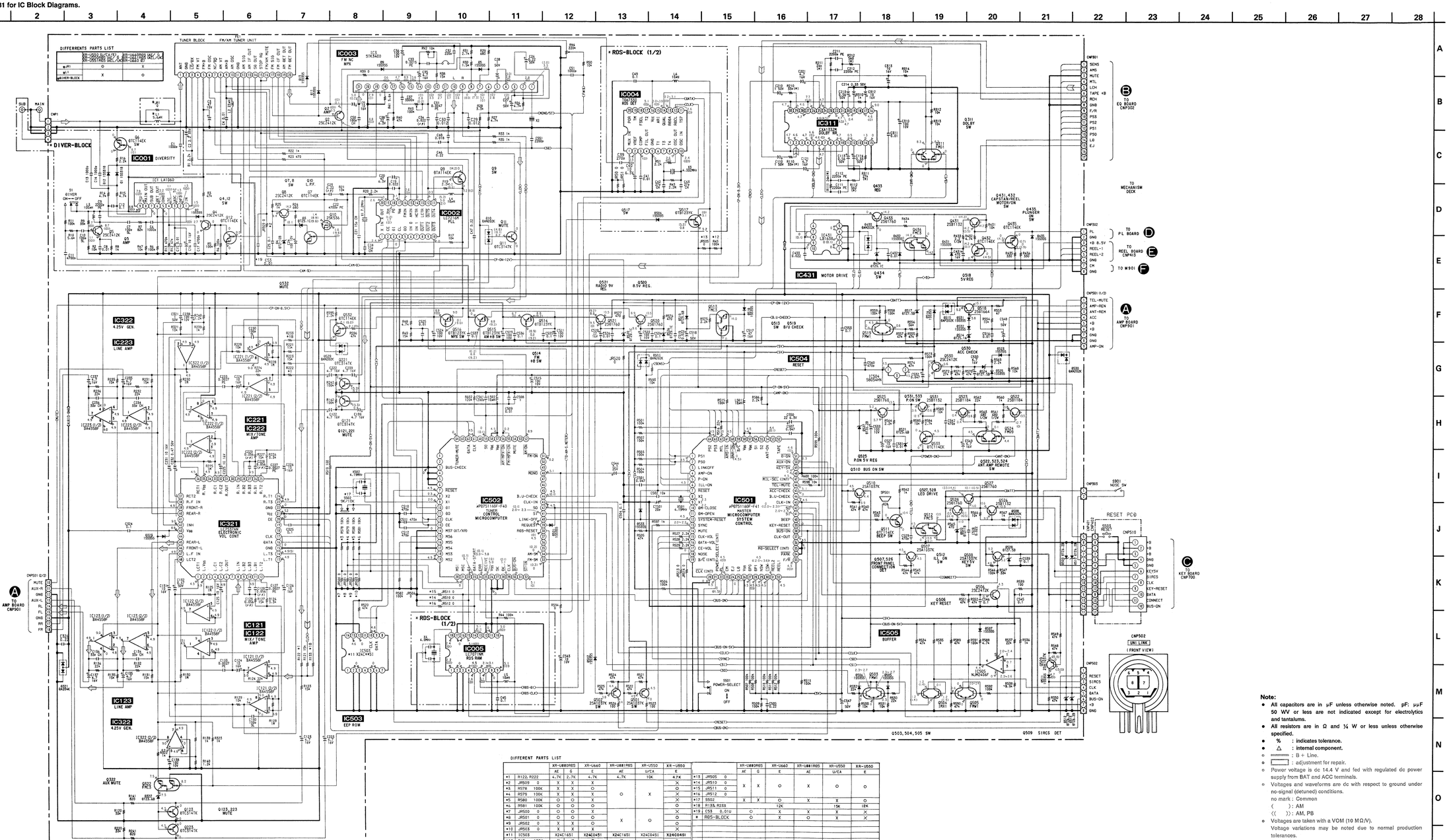
(The other layers' patterns are not indicated.)

Caution:

Pattern face side: (Conductor Side)	Parts on the pattern face side seen from the pattern face are indicated.
Parts face side: (Component Side)	Parts on the parts face side seen from the parts face are indicated.

4-5. SCHEMATIC DIAGRAM (MAIN SECTION)

• See page 31 for IC Block Diagrams.



DIFFERENT PARTS LIST

		XR-U880RDS	XR-U660	XR-U881RDS	XR-U550	XR-U550
		AE	G	E	AE	U/CA	E
*1	R122, R222	4.7K	2.7K	4.7K	4.7K	10K	4.7K
*2	JRS09	0	X	X			X
*5	R578	100K	X	O			O
*6	R579	100K	X	X	O	X	X
*5	RS80	100K	O	O			X
*6	RS81	100K	O	O			O
*7	JRS00	0	O	X			X
*8	JRS01	0	O	O	X	O	O
*9	JRS02	0	X	X			O
*10	JRS03	0	X	X			X
*11	IC503	X24C16S1	X24C04S1		X24C16S1	X24C04S1	X24C04S1
*12	R45	100K	X	O	X	O	O

		XR-U880RDS	XR-U660	XR-U881RDS	XR-U550	XR-U550
		AE	G	E	AE	U/CA	E
*13	JRS05	0					
*14	JRS10	0	X	X	O	X	O
*15	JRS11	0					
*16	JRS12	0					
*17	S502		X	X	O	X	O
*18	R133, R233			12K		15K	12K
*19	CS5	0.01U	O	X	X	X	X
#	RDS-BLOCK		O	X	O	X	X

Note:

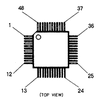
- **All capacitors are in μF unless otherwise noted. pF: μμF 50 WV or less are not indicated except for electrolytics and tantalums.**
- **All resistors are in Ω and ¼ W or less unless otherwise specified.**
- **% : indicates tolerance.**
- **△ : internal component.**
- ═ : B + Line.
- ▭ : adjustment for repair.
- Power voltage is dc 14.4 V and fed with regulated dc power supply from BAT and ACC terminals.
- Voltages and waveforms are dc with respect to ground under no-signal (detuned) conditions.
  no mark : Common
  ( ) : AM
  (( )) : AM, PB
- Voltages are taken with a VOM (10 MΩ/V).
  Voltage variations may be noted due to normal production tolerances.
- Signal path.
  ⇨ : FM ⇨ : PB

• Semiconductor Lead Layouts

LB1638M

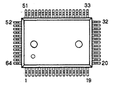
LC7216M

LC7537AN



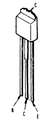
μPD75008GB-632-3B4

μPD75116GF-E40-3BE
μPD75116GF-E41-3BE



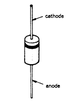
XRA10393F

2SA1184F-R
2SA1385



DTZ10B
DTZ11B
DTZ3.6B
DTZ5.1C
DTZ5.6B
DTZ6.2B
DTZ7.5B
DTZ9.1C
1SS55

1S2472

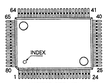


LC7071NM

CXA1332M

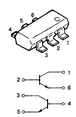
RS20

TC9240F



X24C16SI

IMX1

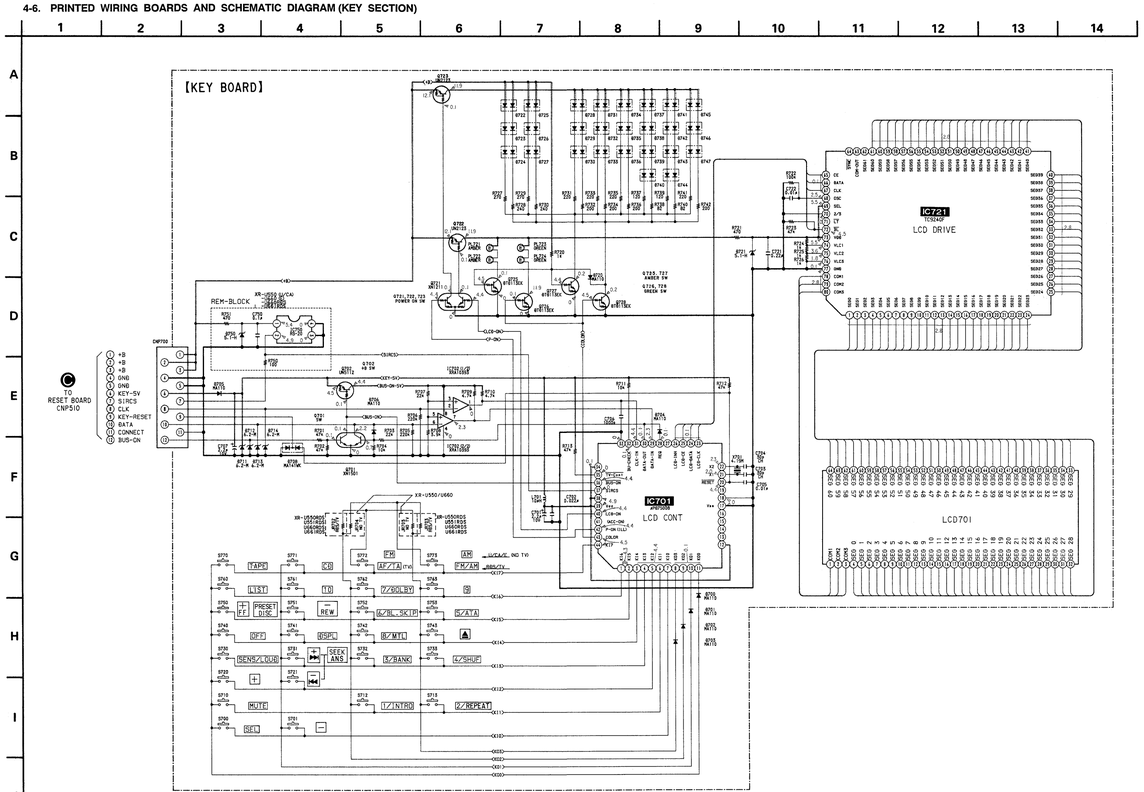


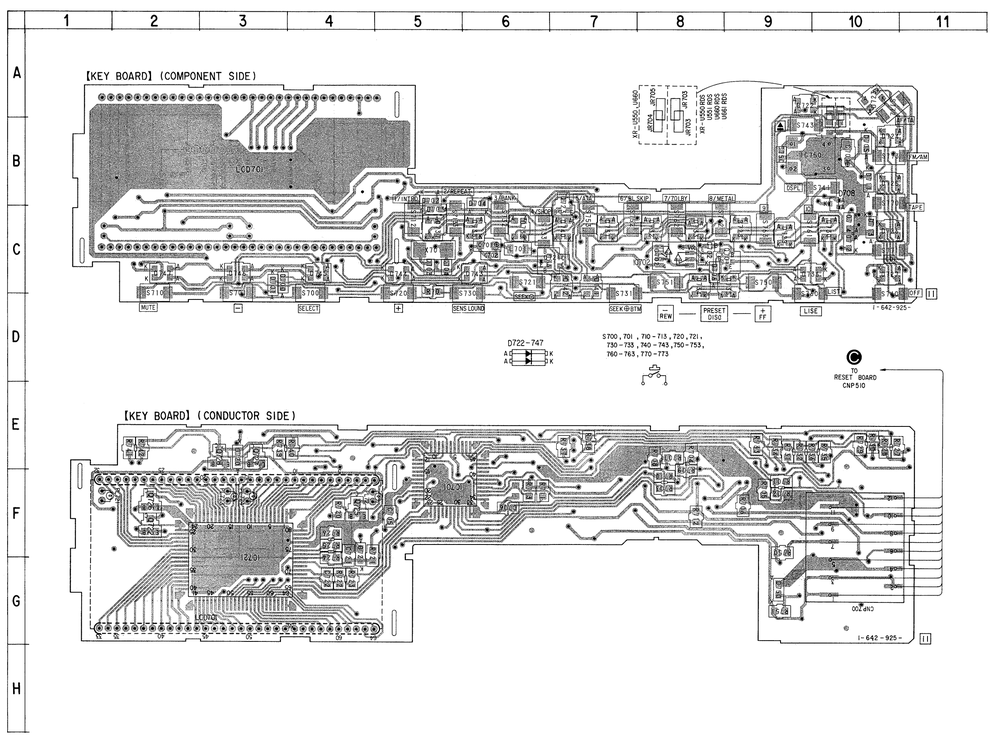
2SD1760F5-Q

MA110
MA8051-H
MA8062-M

CL-155Y/PG-CD

4-6. PRINTED WIRING BOARDS AND SCHEMATIC DIAGRAM (KEY SECTION)





• Semiconductor Location

Ref. No.	Location	Ref. No.	Location
D700	C-3	D737	C-5
D701	C-3	D738	C-6
D702	B-5	D739	C-6
D703	C-5	D740	C-7
D704	B-6	D741	C-7
D705	B-10	D742	C-7
D711	B-10	D743	C-6
D712	C-10	D744	C-5
D713	C-10	D745	C-4
D714	C-10	D746	C-3
D720	E-3	D747	C-2
D721	F-4		
D722	A-9	IC702	C-8
D723	A-10	IC750	B-9
D724	B-10		
D725	B-10	Q701	C-9
D726	C-10	Q702	C-8
D727	C-10	Q721	C-6
D728	C-9	Q722	F-2
D729	C-9	Q723	C-7
D730	C-10	Q725	F-4
D731	C-7	Q726	F-2
D732	C-8	Q727	E-3
D733	C-8	Q728	E-3
D734	C-8		
D735	C-9	IC701	F-5
D736	C-9	IC721	G-3

Note on Schematic Diagram:

- All capacitors are in μF unless otherwise noted. pF: μμF
  50 WV or less are not indicated except for electrolytics and tantalums.
- All resistors are in Ω and ¼ W or less unless otherwise specified.
- % : indicates tolerance.
- ○ ——— : B + Line.
- ○ Power voltage is dc 14.4 V and fed with regulated dc power supply from BAT and ACC terminals.
- ○ Voltages and waveforms are dc with respect to ground under no-signal (detuned) conditions.
  no mark : PB
  ( ) : STOP
- ○ Signal path.
  ∑ : PB

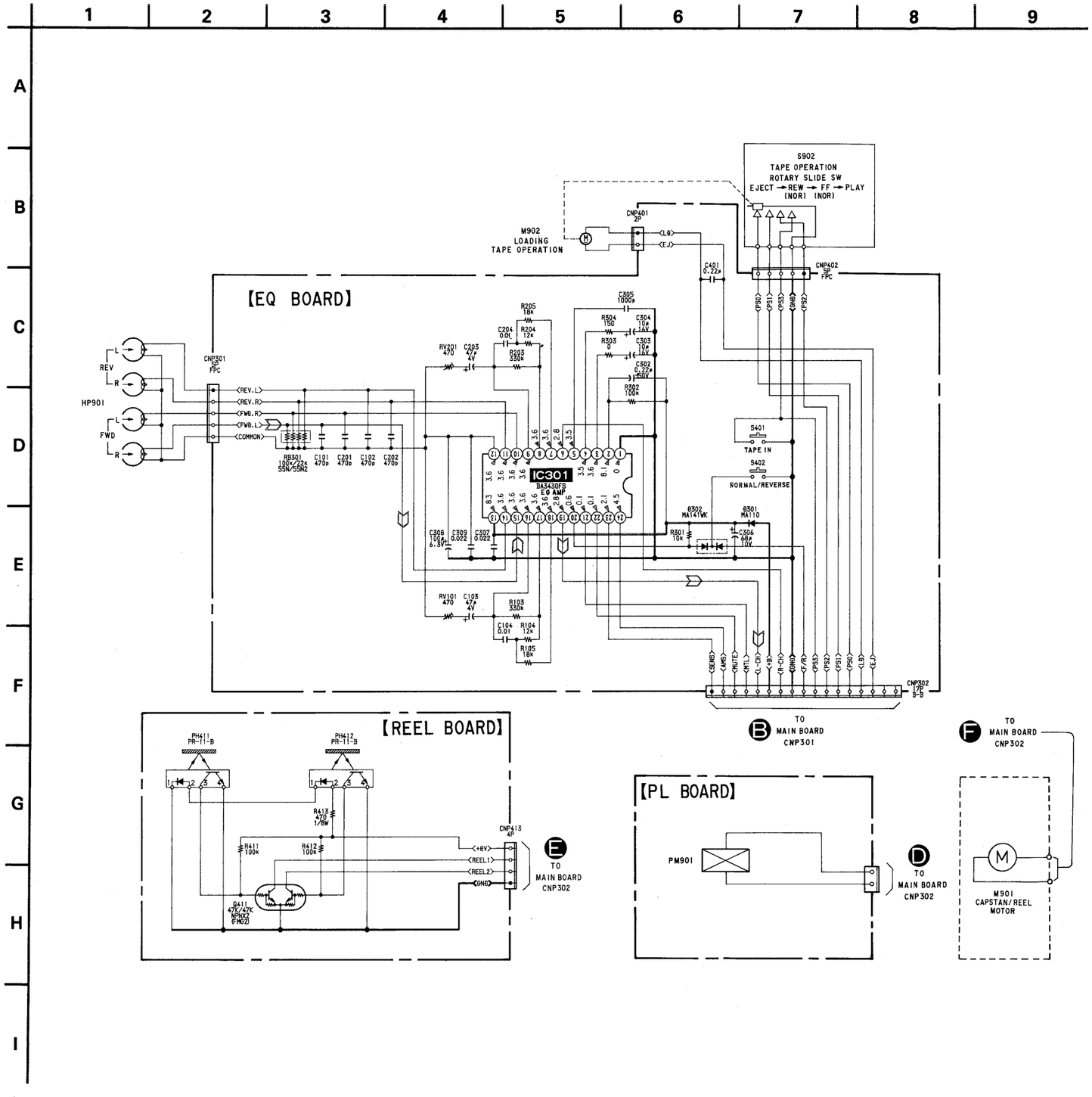
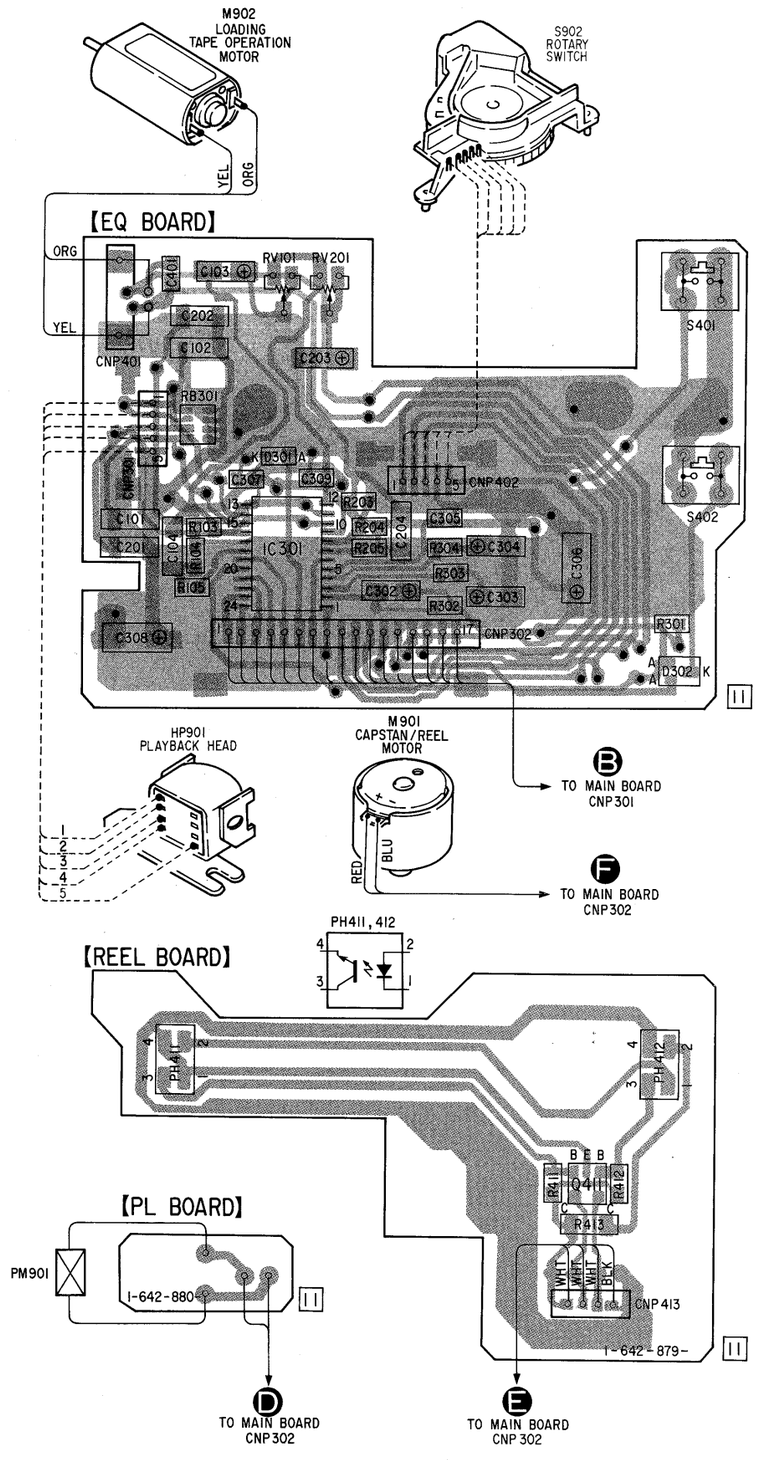
Note on Printed Wiring Board:

- ○——○ : parts extracted from the component side.
- ● : Through hole.
- ▒▒▒ : Pattern from the side which enables seeing.

(The other layers' patterns are not indicated.)

Caution:

Pattern face side: (Conductor Side)	Parts on the pattern face side seen from the pattern face are indicated.
Parts face side: (Component Side)	Parts on the parts face side seen from the parts face are indicated.

4-7. PRINTED WIRING BOARDS AND SCHEMATIC DIAGRAM (EQ, REEL, PL SECTION)

• See page 31 for IC Block Diagrams.